Revision History

Rev	Date	

2 Architecture

2.1 Block Diagram

The link layer is partitioned to two cores, a Link Core and a Host Controller Core. The Link Core is responsible for the communications and operations between the link layer and the physical layer. The Host Controller is responsible for the communications and services between the link layer and a host controller. Only the link core is covered in this specification.

4 Link/PHY Interface Operations

All control and data signals are synchronized to and sampled on the rising edge of SClk.

The Ctl[0:1] control the flow of information and data between the Link Layer and Physical Layer. The encoding of Ctl[0:1] is shown in tables 4.xxx and 4.xxx.