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PCI Express 16-bit VERA Testbench

FEATURES

16 bit PIPE Spec PCI Express Testbench
Link training
Initial Flow Control

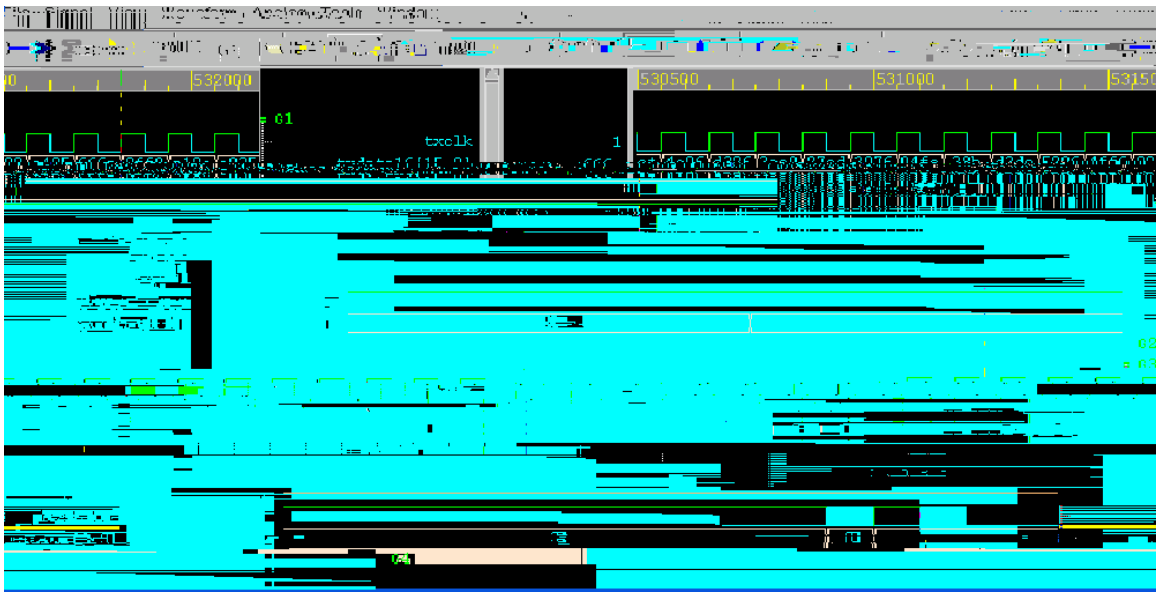

Figure 1 Waveform of Receiver Detect and Power change

Figure 2 Waveform of Training Set Transition from TS1 to TS2

Initial Flow Control

After link up the testbench will generate and receive DLLP initial flow control packets. These packets include initial credits for non-posted, posted and completion credits.

Additional Tasks to be Added

The testbench currently does not include credit updates and credit control. Additional Packet processing including Messages; IOWR; IORD and completion packets. Error Checking, Data compare functions and NACK generation needs to be added Additional PIPE spec functions such as loopback, electrical idles, Serdes errors.