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## Limited Warranty

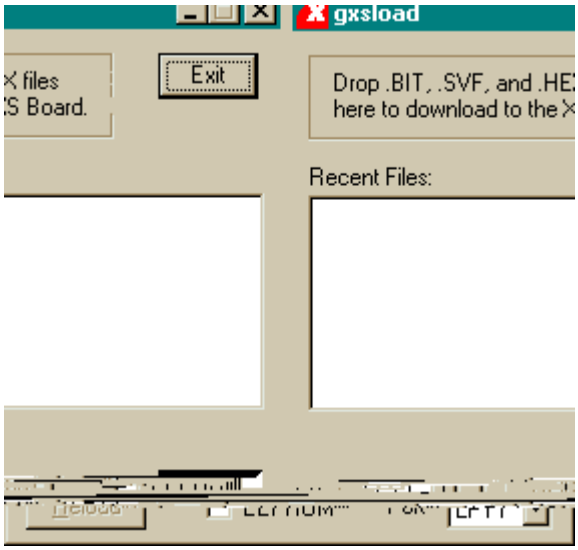
## Table of Contents

# 2

# XSV Overview

The XSV Board brings you the power of the XILINX Virtex FPGA embedded in a framework for processing video and audio signals. The XSV Board has a single Virtex

- Video decoder that accepts NTSC/PAL/SECAM signals through an RCA jack or S-




Your next step is to select the parallel port that your XSV Board is connected to using the

| Flash RAM Pin | Virtex FPGA Pin | XC95108 CPLD Pin |
|---|---|---|
| /RESET | N/A | 3 |

## SRAM Banks

| Direct VGA Pin | RAMDAC Pin | Virtex FPGA Pin | LXT970A Function |
|---|---|---|---|
| | D1 | 41 | |

FPGA and the CPLD. The FPGA acts as a MAC (media access controller) and manages

The CPLD also gets receives the status outputs from the PHY chip that normally drive LEDs. The outputs are active-low and indicate when 100 Mbps operation is selected

| LXT970A Pin | Virtex FPGA Pin | XC95108 CPLD Pin | RAMDAC |
|---|---|---|---|
| /LEDS | | 1 | |
| /LEDR | | 95 | |
| /LEDT | | 96 | |
| /LEDL | | 97 | |
| /LEDC | | 99 | |

| Expansion Connector Pin | Virtex FPGA Pin to Left Connector | Virtex FPGA Pin to Right Connector | SRAM Function |
|---|---|---|---|

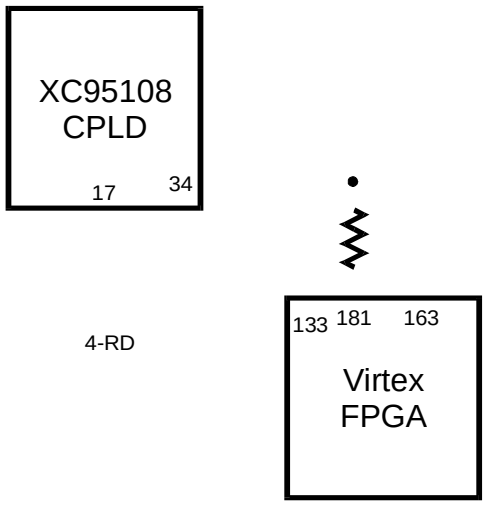
The table below lists the connections from the FPGA and CPLD to the switches. The DIP

| | Virtex FPGA Pin | XC95108 CPLD Pin | Flash RAM Function |
|---|---|---|---|

| LED | Virtex FPGA Pin | XC95108 CPLD Pin | Flash RAM Function |
|---|---|---|---|
| SL5 | 138 | 37 | D5 |


XC95108

If you want to access the JTAG port of the FPGA, all the requisite pins are already connected to the Xchecker interface except for TDO. The TDO pin of the FPGA connects to pin 34 of the CPLD, so you must route the signal through the CPLD and onto the RD pin of the Xchecker interface (which the Xchecker uses for TDO). You must also make sure that pins 133 and 163 on the FPGA are tristated in your design or else they will override TDO.



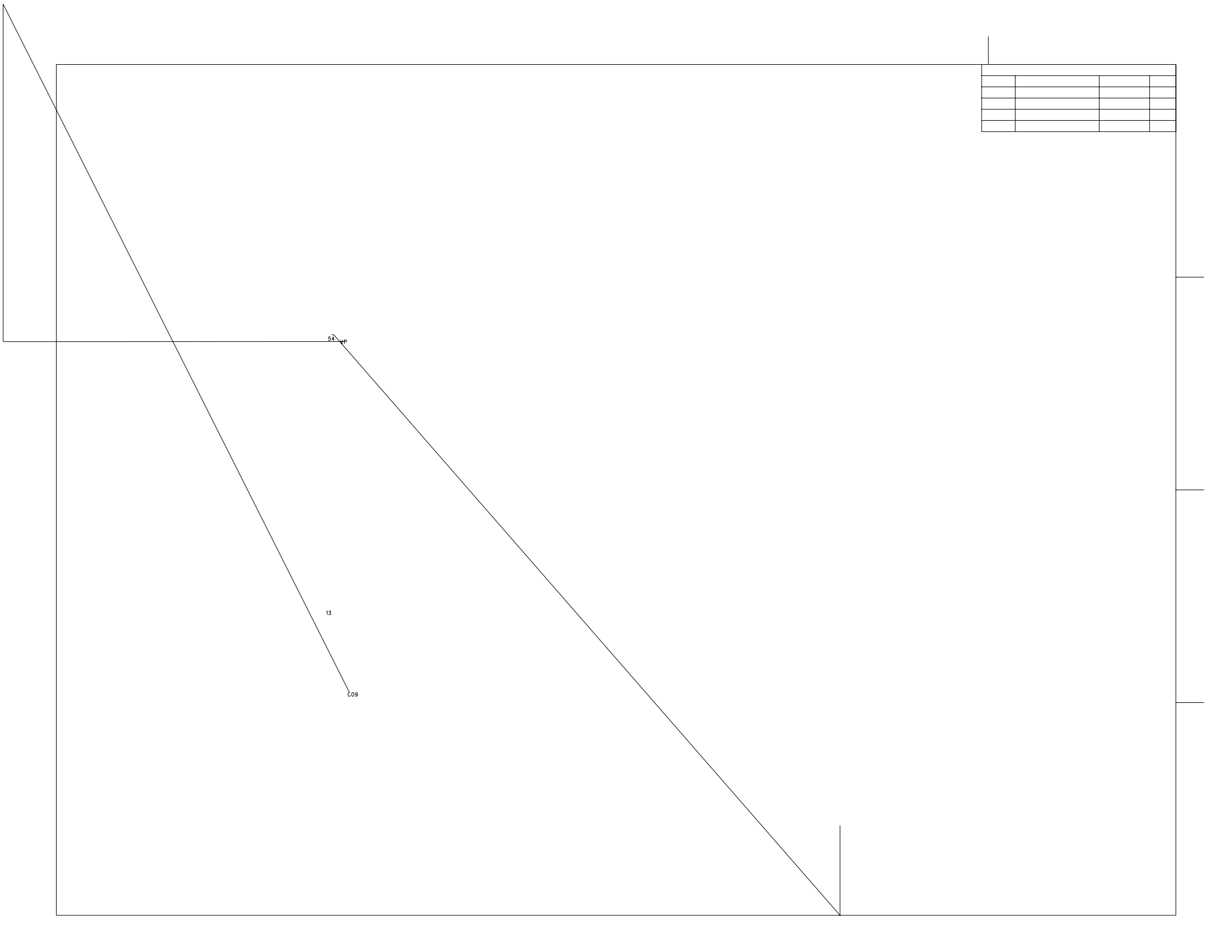
# A

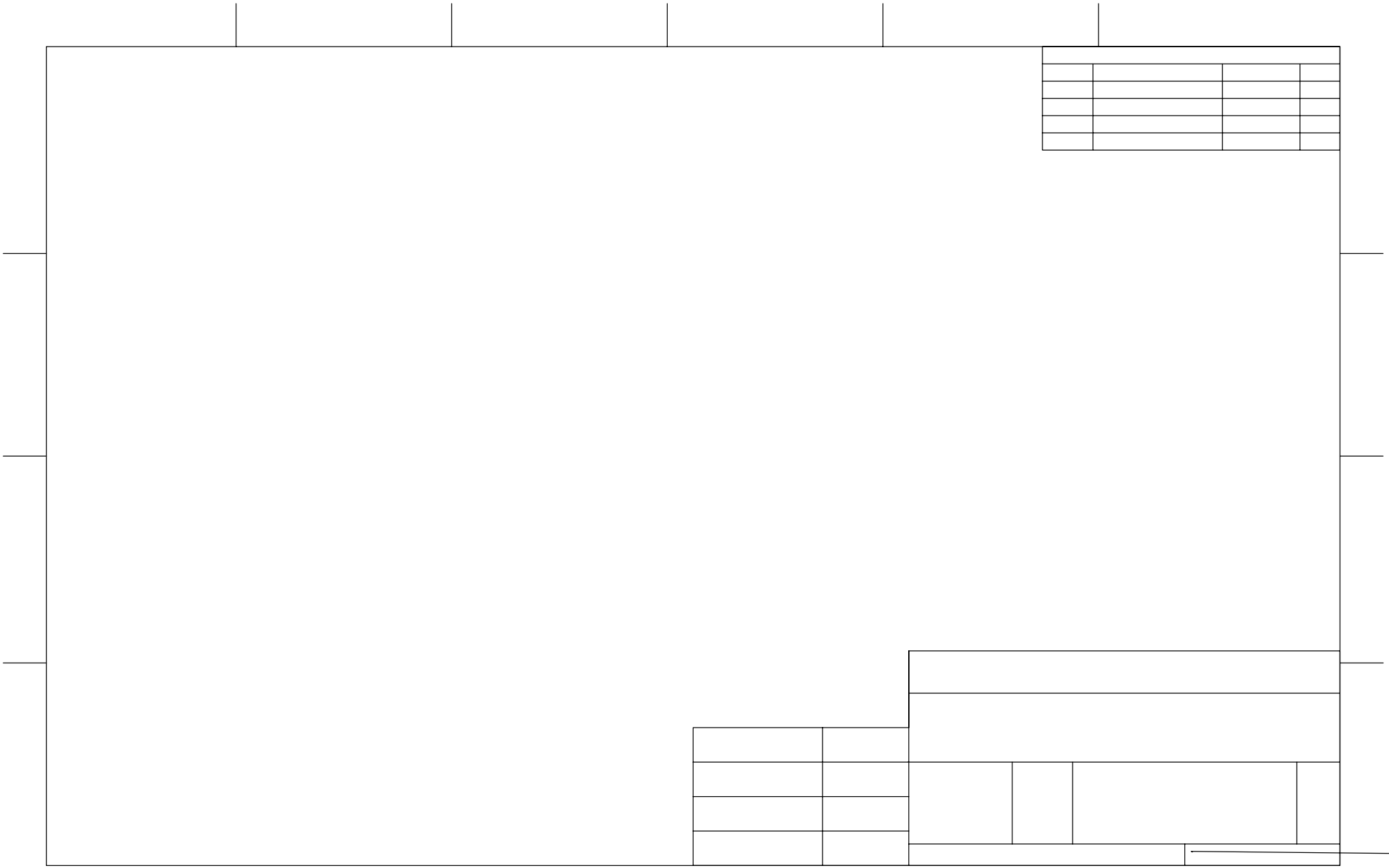
# XSV Pin Connections

The following tables list the pin numbers of the Virtex FPGA and the XC95108 CPLD along with the pin names of the other chips that they connect to. These connections correspond with the pin assignments in the user-constraint files VIRTEX.UCF and CPLD.UCF.

## Connections Between the Virtex FPGA and the Other XSV Board Components4

| Virtex FPGA | | XC95108 CPLD | LEDs | Switches | Flash RAM | Ethernet | Video Decoder | RAMDAC | Codec | RAM | PS/2 | USB | Parallel Port | Serial Port | Prog. Osc. | Xchecker |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | | | | | | | | | | | | | | | |
| 2 | TMS | 35 | S3 (left) | | D3 | | | | | | | | | | | TMS |
| 3 | | | | | | | | | MCLK | | | | | | | |
| 4 | | | | | | | | | LRCK | | | | | | | |
| 5 | | | | | | | | | SCLK | | | | | | | |
| 6 | | | | | | | | | SDIN | | | | | | | |
| 7 | | | | | | | | | SDOUT | | | | | | | |
| 8 | GND | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | VM | | | | |
| 10 | | | | | | | | | | | | VP | | | | |
| 11 | | | | | | | | | | | | RCV | | | | |
| 12 | | | | | | | | | | | | /OE | | | | |
| 13 | | | | | | | | | | | CLK | VPO | | | | |
| 14 | GND | | | | | | | | | | | | | | | |
| 15 | VCCO | | | | | | | | | | | | | | | |
| 16 | VCCINT | | | | | | | | | | | | | | | |
| 17 | | | | | | | | | | | DATA | VMO | | | | |
| 18 | | | | | | FDS/MDINT | | | | | | | | | | |
| 19 | | | | | | MDC | | | | | | | | | | |
| 20 | | | | | | MDIO | | | | | | | | | | |
| 21 | | | | | | CRS | | | | | | | | | | |
| 22 | GND | | | | | | | | | | | | | | | |
| 23 | | | | | | COL | | | | | | | | | | |
| 24 | | | | | | TRSTE | | | | | | | | | | |
| 25 | | | | | | TxEN | | | | | | | | | | |
| 26 | | | | | | RxDV | | RS2 | | | | | | | | |
| 27 | | | | | | TxERR | | | | | | | | | | |
| 28 | | | | | | RxERR | | RS1 | | | | | | | | |
| 29 | GND | | | | | | | | | | | | | | | |
| 30 | VCCO | | | | | | | | | | | | | | | |
| 31 | | | | | | TxD4 | | RS0 | | | | | | | | |
| 32 | VCCINT | | | | | | | | | | | | | | | |
| 33 | | | | | | RxD4 | | | | | | | | | | |
| 34 | | | | | | RxD3 | | D7 | | | | | | | | |
| 35 | | | | | | RxD2 | | D6 | | | | | | | | |
| 36 | | | | | | RxD1 | | D5 | | | | | | | | |
| 37 | GND | | | | | | | | | | | | | | | |
| 38 | | | | | | RxD0 | | D4 | | | | | | | | |
| 39 | | | | | | TxD3 | | D3 | | | | | | | | |
| 40 | | | | | | TxD2 | | D2 | | | | | | | | |
| 41 | | | | | | TxD1 | | D1 | | | | | | | | |
| 42 | | | | | | TxD0 | | D0 | | | | | | | | |
| 43 | VCCINT | | | | | | | | | | | | | | | |
| 44 | VCCO | | | | | | | | | | | | | | | |
| 45 | GND | | | | | | | | | | | | | | | |


54
VP
13
C09



DRAWI

SHEET: